METHOD OF FORMING METAL LINE OF SEMICONDUCTOR DEVICE

BACKGROUND

Field of the Invention

[0001] The present invention relates to a method of forming a metal line of a semiconductor device, and more specifically to a method of forming a metal line of a semiconductor device capable of minimizing damage on an underlying element due to plasma-induced charges accumulated in the metal line in an over-etching process during forming the metal line connected to the underlying element.

Discussion of Related Art

[0002] Generally, a metal line is connected to an underlying element by carrying out a main etching process and an over-etching process using a plasma etching method after depositing a metal layer. During the process of forming the metal line, charges induced by plasma are accumulated in the metal line, which serve as a charging antenna, whereby the charges accumulated in the metal line damage the underlying element.

[0003] Figs. 1A to 1F are cross-sectional views illustrating a conventional method of forming a metal line of a semiconductor device.

[0004] Referring to Fig. 1A, an underlying element 11 is formed on a semiconductor substrate 10. The underlying element 11 includes all unit elements employed in the present invention.

[0005] Referring to Fig. 1B, an interlayer insulating film 12 is formed on the semiconductor substrate 10 including the underlying element 11. A metal line contact hole 13 is formed by etching a portion of the interlayer insulating film 12 to expose a portion of a top surface of the underlying element 11.

[0006] Referring to Fig. IC, conductive materials fill an inner portion of the metal line contact hole 13, so that a metal line plug 14 is formed to be connected to the underlying element 11.

[0007] Referring to Fig. 1D, a metal layer 15 is formed on the interlayer insulating film 12 including the metal line plug 14. A photoresist pattern 16 is formed on the metal layer 15 to cover a portion, in which the metal line is formed, including a top surface of the metal line plug 14.

[0008] Referring to Fig. 1E, a main etching process is carried out using a plasma etching method to etch the exposed portion of the metal layer 15.

[0009] Referring to Fig. 1F, the metal line 150 connected to the metal plug 14 is formed by carrying out an over-etching process for eliminating the metal layer 15, which remains even after performing the main etching process.

[0010] In processes mentioned above, charges induced by plasma during the main etching process using the plasma etching method are accumulated in the metal layer 15. In the main etching process, the plasma-induced charges do not damage the underlying element because the metal layer 15 on a wafer is electrically connected, not isolated. However, since the metal line 150 formed by the over-etching process is completely isolated not electrically connected, the metal line 150 serves as a charging antenna, so that the charges accumulated in the metal line 150 during the main etching process and the over-etching process electrically damage the underlying element 11 to deteriorate reliability thereof. When a multi-layer metal line is formed, damage on the underlying element 11 due to the charges is significantly increased because the aforementioned plasma damage is repeatedly accumulated.

[0011] Damage on the underlying element 11 due to the plasma-induced charges is affected by a layout of an antenna structure of the metal line 150, which is disclosed in Journal of the Korean Physical Society, Vol. 35, December 1999, pp. S742 to S746, entitled "Effect of Plasma Induced Charging in Interconnect Metal Etch on the Characteristics of a Ferroelectric Capacitor".

SUMMARY OF THE INVENTION

[0012] Accordingly, the present invention is directed to provide a method of forming a metal line of a semiconductor device, capable of improving electrical efficiency and reliability of the semiconductor device by minimizing damage on an underlying element connected to the metal line due to plasma–induced charges accumulated in the metal line during forming the metal line.

[0013] One aspect of the present invention is to provide a method of forming a metal line of a semiconductor device, comprising the steps of: preparing a semiconductor substrate comprising an underlying element and forming an interlayer insulating film thereon; forming a metal line contact hole to expose a portion of the underlying element, and a metal fuse contact hole to expose a portion of the semiconductor device by etching a portion of the interlayer insulating film; forming a metal line plug and a metal fuse plug by filling the metal line contact hole and the metal fuse contact hole with conductive materials, respectively; forming a metal layer on the interlayer insulating film including the metal line plug and the metal fuse plug; forming a metal line pattern and a metal fuse pattern electrically connected to the metal line pattern by etching the metal layer by, for example, means of a main etching process and an over-etching process for forming the metal line; and forming the metal line by electrically isolating the metal line pattern and the metal fuse pattern by means of the over-etching process to the metal fuse.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

[0015] Figs. 1A to 1F are cross-sectional views illustrating a conventional method of forming a metal line of a semiconductor device; and,

[0016] Figs. 2A to 2G are cross-sectional views illustrating a method of forming a metal line of a semiconductor device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0017] Now, preferable embodiments according to the present invention will be described in detail with reference to the appended drawings. However, the present invention is not limited to the embodiments disclosed in the following description, but can be implemented into various changes and modifications. Thus, these embodiments according to the present invention are intended to completely inform those skilled in the art of a scope of the present invention.

[0018] Figs. 2A to 2G are cross-sectional views illustrating a method of forming a metal line of a semiconductor device according to an embodiment of the present invention.

[0019] Referring to Fig. 2A, an underlying element 21 is formed on a semiconductor substrate 20. The underlying element 21 includes all unit elements employed in the semiconductor device.

[0020] Referring to Fig. 2B, an interlayer insulating film 22 is formed on the semiconductor substrate 20 including the underlying element 21. A metal line contact hole 23L for exposing a portion of a top surface of the underlying element 21 and a metal fuse contact hole 23F for exposing a portion of the semiconductor substrate 20 are formed by etching a portion of the interlayer insulating film 22, respectively.

[0021] Referring to Fig. 2C, a metal line plug 24L connected to the underlying element 21 and a metal fuse plug 24F connected to the semiconductor substrate 20 are formed by filling the metal line contact hole 23L and the metal fuse contact hole 23F with conductive materials, respectively.

[0022] Referring to Fig. 2D, a metal layer 25 is formed on the interlayer insulating film 22 including the metal line plug 24L and the metal fuse plug 24F. A photoresist pattern 26 is formed on the metal layer 25. The photoresist pattern 26 is formed to cover a metal line area including the metal line plug 24L and a metal fuse area including the metal fuse plug 24F and to have a narrow space between the metal line area and the metal fuse area where etch loading effect is exhibited at the time of performing a main etching process and an over-etching process for forming the metal line. On the other hand, the photoresist pattern 26 formed in the metal fuse area may be multiple patterns. At that time, spaces between the multiple patterns must be narrow enough to exhibit etch loading effect.

[0023] Referring to Fig. 2E, in order to etch the exposed portions of the metal layer 25, the main etching process using the plasma etching method is carried out.

[0024] Referring to Fig. 2F, the over-etching process is carried out to eliminate the metal layer 25, which remains even after performing the main etching process, whereby a metal line pattern 25F connected to the metal line plug 24L is formed and at least one metal fuse pattern 25F connected to the metal fuse plug 24F is formed. Space between the metal line pattern 25L and the metal fuse pattern 25F is set such that the metal layer 25 having a constant thickness remains in the space even after performing the over-etching process, due to etch loading effect. Thus, the metal line pattern 25L and the metal fuse pattern 25F is electrically connected to each other. Further, where there are a plurality of metal fuse patterns 25F, the metal fuse patterns 25F are densely formed and the metal layer 25 having a constant thickness between the patterns remains, so that the metal fuse patterns 25F are electrically connected to each other. Therefore, the underlying element 21, the metal line plug 24L, a metal line pattern 24F, the metal fuse pattern 25F, the metal fuse plug 24F and

the semiconductor substrate 20 are electrically connected sequentially. At this time, the metal fuse plug 24F and at least one metal fuse pattern 25F serves as a metal fuse 245.

[0025] Referring to Fig. 2G, the over-etching process to the metal fuse is carried out to eliminate the metal layer 25, which remains on the periphery of the metal fuse pattern 25F, so that the metal fuse 245 and a metal line 250 electrically isolated from the metal fuse are formed.

[0026] In the aforementioned processes, charges induced by plasma during the main etching process using the plasma etching method of forming the metal line 250 are accumulated in the metal layer 25. In the main etching process, since the metal layer 25 on a wafer is electrically connected, not completely isolated, the plasma-induced charges do not damage the underlying element 21 (see Fig. 2E). The metal line pattern 25L formed in the over-etching process following the main etching process is isolated from an adjacent metal line pattern (not shown), while one side of the metal line pattern 25L is connected to the metal fuse 245, as shown in Fig. 2F, so that the charges accumulated in the metal line pattern 25L during the main etching process and the over-etching process are discharged into the semiconductor substrate 21 through the metal fuse 245. Accordingly, the plasma-induced charges do not damage the underlying element 21. As shown in Fig. 2G, the plasma-induced charges are accumulated in the metal line 250 and the metal fuse 245 during the over-etching process for the metal fuse and plasma-induced charges can damage the underlying element 21. However, the level of damaging is not significant compared to the conventional method of forming a metal line. In other words, in the conventional method, the accumulated charges damage the underlying element during the main etching process and the over-etching process for forming the metal line, but in the method according to the present invention, the over-etching process for the metal fuse, only. Therefore, the damage due to the charges is insignificant.

[0027] Although, a structure of a single layer metal line is described in the embodiment of the present invention, it is possible to minimize damage of the underlying element due to the plasma-induced charges by forming a multi-layer metal line using the same method. When a principle of the present invention applies to the multi layer metal line, there are more or less differences in components, for example, another metal line is formed on the metal line 250 of Fig. 2G and another metal fuse is formed on the metal fuse of Fig. 2G or the like, but the multi layer metal line can be easily implemented by those skilled in the art. Accordingly, the present invention is not limited to the embodiment described referring to the appended drawings, but includes all the methods of forming a metal line of a semiconductor device, capable of employing the principle of the present invention.

[0028] As described above, according to the present invention, when the metal line is formed, the metal fuse connected to the metal line and the semiconductor substrate is formed at the same time, so that the plasma-induced charges accumulated in the metal line during the process of forming the metal line are discharged into the semiconductor substrate through the metal fuse. Therefore, it is possible to improve electrical efficiency and reliability of the element by minimizing damage to the underlying element connected to the metal line.